Volume 46, Number 2, 2005 **ACTA TECHNICA NAPOCENSIS**
Electronics and Telecommunications

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I. INTRODUCTION

The 723 IC is a flexible, easy-to-use voltage regulator with excellent performances [1]. It is really a power supply kit, containing temperature-compensated voltage reference V_{REF}, differential amplifier, series pass transistor, Zener diode and current-limiting protective circuit. Using some external components the versatile 723 IC can be use to build a large variety of fixed and adjustable regulated voltage: basic low voltage regulator, basic high voltage regulator, positive and negative voltage regulator, positive and negative floating regulator, positive and negative switching regulator [2].

A particular attention should be paid if we want to build a positive voltage regulator adjustable from zero, as long as in the datasheet the adjustable output voltage is from 2V to 37V [2]. One solution uses two 723 ICs and an extra negative input voltage source [3].

The purpose of this paper is to analyze a solution that use only one 723 IC to build an adjustable from zero voltage regulator. We started with one initial circuit configuration and using SPICE simulations we improved it to the final configuration. Our idea has three distinct characteristics:

- keeps the output of the error amplifier above 2V, using the built-in Zener diode;
- keeps both inverting and non-inverting inputs of the error amplifier above 2V even for zero output voltage using resistive voltage dividers between reference voltage and output voltage and respectively between reference voltage and ground;
- uses a "smart" ballast equivalent resistance with a low value for minimum output voltage but with a high value for higher output voltages.

The remainder of the paper is organized as follows. Section II presents the internal simplified structure of 723IC, the basic circuit for the low voltage regulator and the existing solution for a zero volts adjustable from zero voltage regulator using two 723ICs. In Section III our idea is presented using only 723IC and no auxiliary negative voltage source. By means of SPICE simulation we analyze the behavior and performances of each circuit configurations. Section IV is concerned with the validation of our final circuit. We compare its regulation performances with the regulation performances of the existing solution. The regulation performances are obtained by SPICE simulation for both regulators. Finally, some conclusions are drawn in Section V.

II. THE EXISTING SOLUTION FOR ZERO LEVEL ADJUSTMENT

The equivalent circuit of LM 723 is presented in Fig.1. [2].

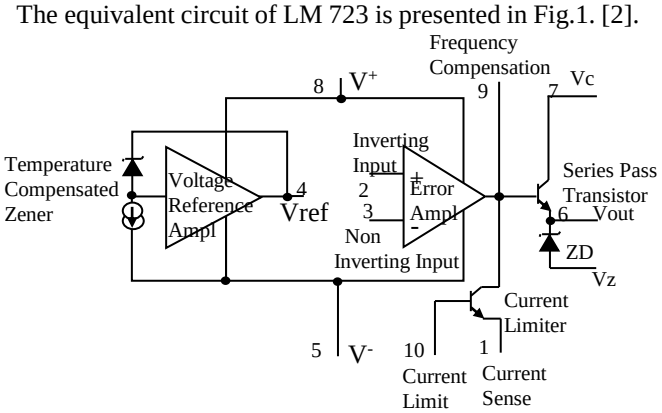

Fig.1. The LM723 voltage regulator

We can see that the V_{REF} appears from pin 4 to pin 5, the same with the negative supply pin of error amplifier (V^-). The well known basic low voltage regulator in the range $V_O \in [2V; V_{REF}]$ is presented in Fig.2.

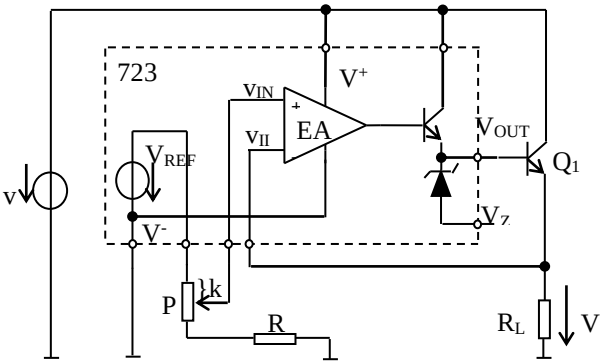

Fig.2. The low voltage regulator

The internal LM 723 structure is still simplified: V_{REF} is represented as a voltage source and the internal current limiter transistor is omitted. The expression of V_O is:

$$V_O = \frac{(1-k)P + R}{P + R} V_{REF} \qquad (1)$$

The P, R voltage divider is sized to provide $V_{Omin} = V_{IN} = V_{II} \leq 2V$. As we know this is necessary to assure enough voltage to keep a series of bipolar transistor (not shown in Fig. 2) inside of IC in their active region for a proper operation of the error amplifier.

So, we cannot use the circuit in Fig.2. to adjust the output voltage to zero as long as we must keep the voltages to the inputs and output of the error amplifier (EA) greater to at least 2V than the potential of its negative supply V^-.

The known solution [3] for zero volts adjustment using 723 IC uses the main idea to connect the negative supply of the amplifier (V^-) to a negative potential, less or equal with -2V. The principle of this solution is illustrated in Fig.3.

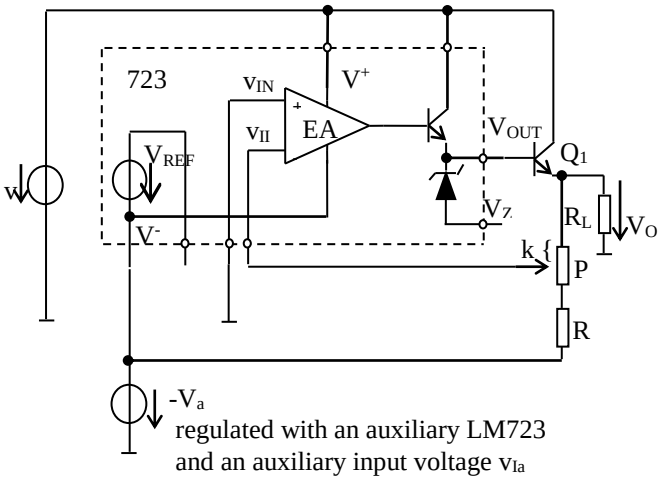

Fig.3. The zero volts adjustment voltage regulator with two 723ICs

The auxiliary negative voltage $-V_a$ is regulated with an auxiliary LM 723 (not shown in Fig.3) having as input an auxiliary negative floating unregulated voltage supply v_{Ia}. V_O can be easily deduced as:

$$V_O = -\frac{kP}{(1-k)P + R}(-V_a) = \frac{kP}{(1-k)P + R} V_a \qquad (2)$$

For $k = 0$, $V_O = 0V$.

The disadvantage of this scheme is its complexity meaning the auxiliary voltage regulator to regulate $-V_a$ and the auxiliary input voltage source.

III. OUR SOLUTION

Our idea is to build a simpler voltage regulator, adjustable from zero, using only one 723 IC and no auxiliary negative voltage source.

III. 1. The initial circuit configuration

In order to prevent the inputs and output of the error amplifier to reach values below 2V we propose the initial circuit configuration presented in Fig. 4.

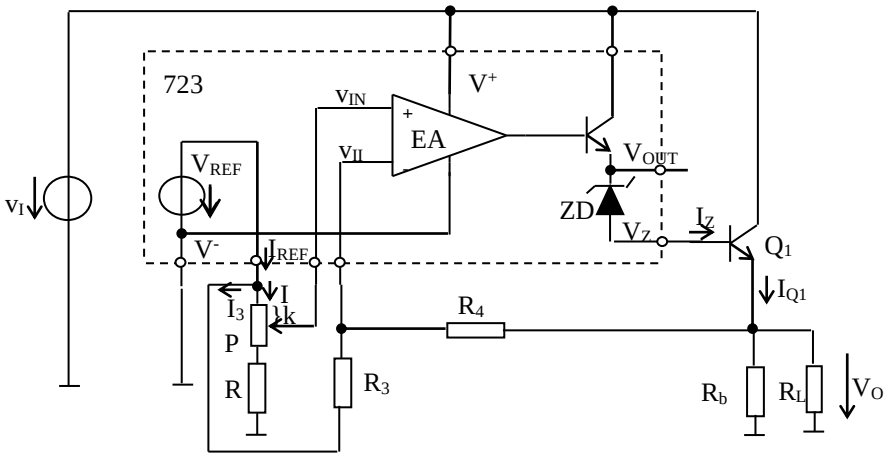

Fig.4. The initial circuit configuration

We use the integrated Zener diode ZD taking the output from the anode of the ZD instead from the emitter of integrated transistor. This way even for $V_O = 0V$ the output of the error amplifier has a potential raised with $V_Z + V_{BE,on} + V_{BE,on1}$ in respect with the V^- potential. As long as $V_Z \approx 6V$, the output of the error amplifier is well solved, with the condition to keep ZD in its regulated region, meaning enough I_Z current. This is why we need a ballast resistor R_b to assure a path for the I_{Q1} current (so implicitly for I_Z current), even in the absence of the load.

The negative feedback is assumed by the R_3, R_4 voltage divider, with its intermediate point connected to the inverting input of the error amplifier. The trick here is we do not connect the end of the divider to the ground, but to a positive stabilized voltage, V_{REF}. All we have to do further is to size the R_3, R_4 divider so that $V_{II} \geq 2V$ for $V_O = 0V$.

The V_O expression is straightforward to deduce:

$$V_O = V_{REF}\left[\frac{(1-k)P+R}{P+R}\cdot\frac{R_3+R_4}{R_3}-\frac{R_4}{R_3}\right] \quad (3)$$

For $k = 0$, $V_{IN} = V_{II} = V_{REF}$, so voltage drop across R_3, so $V_O = V_{REF}$.

For $k = 1$ we expect $V_O = 0V$. From relation (3) results:

$$\frac{R}{P+R} = \frac{R_4}{R_3+R_4} \quad (4)$$

and also from condition of $v_{IN} = V_{II} \geq 2V$ for worst case situation ($V_{REF} = V_{REFmin}$):

$$\frac{P}{P+R}V_{REF\,\min} \geq 2V \quad (5)$$

When we adjust the output voltage, the I_3 current will vary, so in order to keep constant V_{REF}, meaning constant I_{REF} (see data sheet) we place the condition: $I > 10 \cdot I_3$, or:

$$R + P < \frac{1}{10}(R_3 + R_4) \quad (6)$$

An extra design equation can be obtained by imposing the current through V_{REF} (less than 15mA according to the data sheet). For $I_{REF} \approx 5mA$ the following relation appears:

$$\frac{V_{REF}}{R+P} = 5mA \quad (7)$$

Using the design equation (4) - (7) we sized the resistances: I = 1KΩ, I = 410Ω, I = 20KΩ andI = 8.2KΩ.

In order to analyze the behavior of the proposed configuration we conducted some SPICE simulations for different ballast resistance. The numerical results are presented in Table 1.

Table 1

	k	R_b	V_O [V]	V_{OUT} [V]	I_{Q1}
1.	1	1KΩ	0.1182	6.390	1.8μA
2.	0	1KΩ	7.1632	13.8690	14.3mA
3.	1	100Ω	0.0253	6.4435	40.66μA
4.	0	100Ω	7.1663	13.9580	78.84mA
5.	1	10Ω	0.0047	6.5064	233μA
6.	0	10Ω	7.1666	14.0850	724mA

We can see that the minimum output voltage V_O and the current through the external pass transistor I_{Q1} depends on the R_b value. Also from all R_b and k values we can see that the value of V_{OUT} demonstrates that the Zener diode is in its regulation region. In order to obtain the lowest possible output voltage ($k = 1$) we must have a low value of R_b. For $R_b = 10Ω$, k=1, $V_{Omin} = 4.7$ mV (row 5). It is a small enough value to consider that output voltage V_O can be adjusted down to zero. When we set $k = 0$, $V_{Omax} = 7.166$ V (row 6) the current through Q_1 is very high $I_{Q1} = 724$ mA. This is not acceptable, because it is not a useful current, it increases very much the current consumption from the input source. For a higher R_b value, $R_b = 1$ KΩ (for $k = 0$), the maximum I_{Q1} current decreases to 14.3mA (row 2), still a high value, but the minimum output voltage increases up to 118.2 mV (row 1). The V_{Omin} increases with R_b because the I_3 current must flow through R_b resistor.

One solution to decrease V_{Omin} can be to decrease I_3 currentby increasing R_3 and R_4 resistances. Anyway we can not decrease to much the I_3 current because it can reach a level comparable with the input bias current of error amplifier, so the R_3, R_4 will not act anymore as a simple voltage divider.

Returning to R_b we can state: we need a low R_b value when we set minimum V_O but we need a high R_b value when we set higher V_O. So, we need a "smart" resistor that "know" when V_O is very low or high.

III.2. Improved configuration

As a "smart" resistor we use the group R_b, Q_2, Q_3, R_1 and R_2 as one can see in Fig.5.

How does this group work? When k is set towards 1 V_O has a high value (towards V_{REF}). The Q_3 transistor goes into saturation and by the way of consequence Q_2 is off. So, the equivalent ballast resistance is formed by R_b in parallel with R_2 plus the equivalent base-emitter d.c. resistance of Q_3. With appropriate resistors value we can set a high enough equivalent resistance.

When V_O decreases, the base current of Q_3 also decreases and Q_3 moves from the saturation towards the active region. At one moment (depending on the R_1 and R_2 values) Q_3 will be in its active region. When V_O decreases below approximately 0.6V Q_3 will be turned off. On the other hand when Q_3 is not saturated, Q_2 can enter in the active region and draw a nonzero I_{Q2} current from the output. When V_O drop below 0.2V Q_2 enters in saturation, so it has a very low collector-emitter equivalent resistance and in conclusion very low ballast resistance.

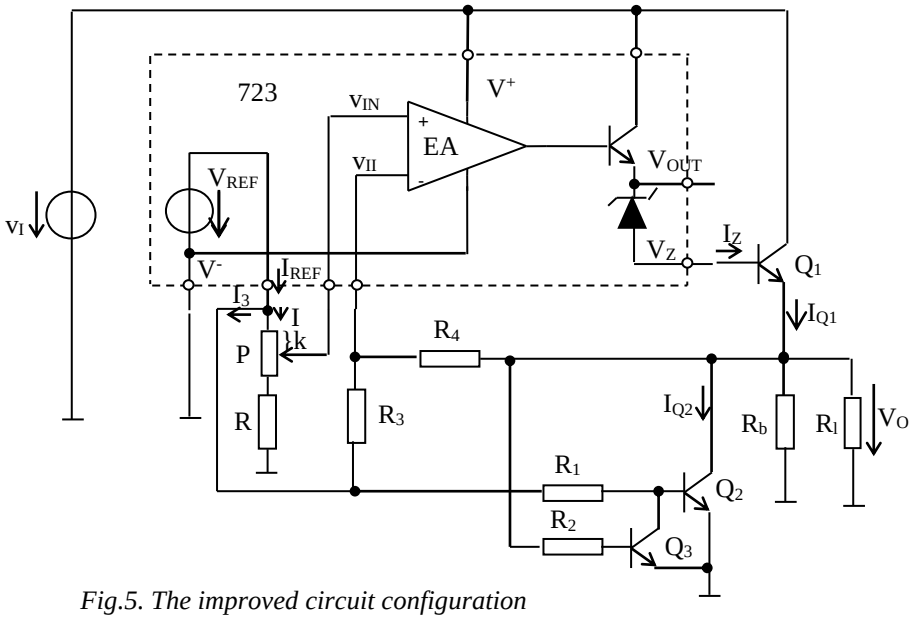

Fig.5. The improved circuit configuration

We simulated this circuit for different combinations of the R_1 and R_2 values. The results are presented in Table 2.

Table 2

	k	R_1 [K]	R_2 [K]	V_O [V]	V_{OUT} [V]	I_{Q1}
1.	1	10	10	0.0151	6.4813	111μA
2.	0	10	10	7.1563	13.7830	2.89mA
3.	0.93	10	10	0.5138	7.3380	155.1mA
4.	1	1	10	0.0109	6.54107	420μA
5.	0	1	10	7.0644	13.6900	2.85mA
6.	0.88	1	10	0.8552	7.7451	490.1mA
7.	1	10	1	0.0151	6.4813	111.1μA
8.	0	10	1	7.1562	13.8360	8.661mA
9.	0.93	10	1	0.5138	7.3380	155mA

From Table 2 one can observe we can obtain very low values of V_O (15mV, 10mV, for $k = 1$) and also the I_{Q1} value are acceptable (2.9mA or 8.6mA) for V_{Omax} ($k = 0$). The equivalent ballast resistance behaves as we expected: low value for V_{Omin} and high value for V_{Omax}.

A parametric analysis of I_{Q1} value as a function of k value (V_O value) show us that the maximum I_{Q1} current appears at a V_O value for that the Q_2 transistor is in the active region. For example in rows 3 and 9 for $k = 0.93$, $V_O = 514$ mV results $I_{Q1} = 155$ mA. Or even worse I_{Q1} reaches 490 mA for $R_1 = 1\text{K}\Omega$, $R_2 = 10\text{K}\Omega$, $k = 0.88$, $V_O = 855$ mV.

We have solved one problem (we reduced to an acceptable level the I_{Q1} for V_{Omax}) but a new problem appears: high I_{Q1} value for a certain V_O value (depending on R_1 and R_2 values). The high I_{Q2} value appears for active region of Q_2 as a consequence of the collector current I_{Q2}. This value is:

$$I_{Q2} = \beta \cdot \frac{V_{REF} - V_{BEon2}}{R_1} \qquad (8)$$

where β is the d.c. current gain of the Q_2 transistor.

One way to reduce I_{Q2} is to increase R_1, but doing this we increase the V_{Omin} (10.9 mV for $R_1 = 1\text{K}\Omega$, 15.1 mV for $R_1 = 10\text{K}\Omega$), so this is not a very good idea.

A better idea is to use a transistor with a low β value, the idea that is analyzed in the next paragraph.

III.3. The final configuration

We know that a transistor can be also used in the reverse active region, where its current gain β_R is much smaller that the one in the active region. So, the great idea is to reverse the Q_2 transistor so that when in active reverse region it will work with a very low current gain.

Table 3

	k	R_1 [K]	R_2 [K]	V_O [V]	V_{OUT} [V]	I_{Q1}
1.	1	10	10	0.0082	6.4451	824nA
2.	0	10	10	7.1565	13.7830	2.896mA
3.	0.93	10	10	0.5077	7.0904	1.241mA
4.	1	1	10	0.0109	6.5190	266μA
5.	0	1	10	7.0644	13.6900	2.855mA
6.	0.93	1	10	0.5042	7.208	14.73mA
7.	1	10	1	0.0082	6.4451	60.1μA
8.	0	10	1	7.1564	13.8370	8.66mA
9.	0.93	10	1	0.5077	7.0904	1.241m
10.	1	10	50	0.0067	6.2849	2.12u
11.	0	10	50	7.1566	13.7730	2.379m
12.	0.93	10	50	0.4349	7.0168	1.241m

The final, complete scheme is shown in Fig.6. The extra potentiometer P_Z is necessary to make the zero volts adjustment.

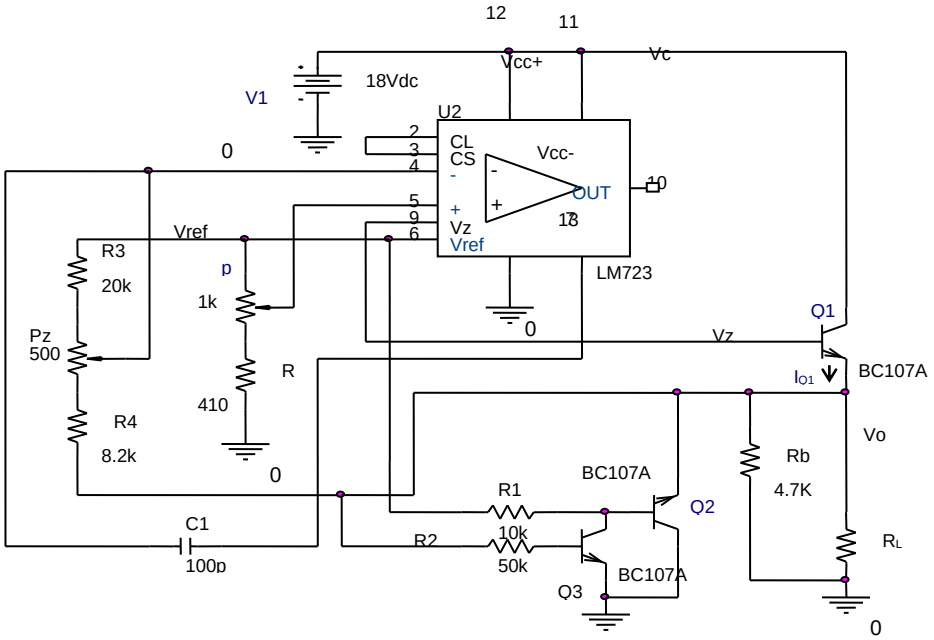

Fig. 6. The adjustable from zero voltage regulator

In Table 3 some numerical results obtained by SPICE simulation for different R_1 and R_2 values combination are presented.

The numerical results show good performance of our adjustable from zero voltage regulator. Regardless the R_1 and R_2 values the V_{Omin} has a very good value, less than 10 mV (even 6.7 mV, in row 10). This value can be considered as low as zero for a voltage regulator. The maxim value of the I_{Q1} current is below 3 mA in all but one situation, so no important extra current for proper operation of voltage regulator is necessary.

We can observe the drastically reduction of maximum I_{Q1} due to the operation of Q_2 in reverse region. For example, for $R_1 = R_2 = 10K\Omega$ and $k = 0.93$, I_{Q1} was reduced from 155 mA with Q_2 in forward active region (row3 in Table 2) up to 1.24 mA with Q_2 in reverse active region (row3 in Table 3). It is important to note that the maximum I_{Q1} current appears for V_{Omax} when Q_2 is saturated, not for Q_2 in active region. This happens for all situations where $R_1 \neq 1K\Omega$.

As optimal solution we choose the last one in Table 3, R_1=10KΩ, R_2=50KΩ that provide V_{Omin}=6.7 mV and I_{Q1max}=2.38 mA.

The final version of the voltage regulator was also practically implemented. For better results, a small adjustment was necessary for the R_1 resistor value (8.2KΩ instead of 10KΩ). The experimental results are presented in Table 4.

The minimum output voltage V_{Omin}=2.8mV is even better than the value obtained by simulation (6.7mV). The maximum output voltage V_{Omax}=7.073V is quite the same with the simulated one (7.1566V). For the maximum output voltage the current through Q_1 is 1.57 mA, meaning low current necessary for the equivalent ballast resistor. The voltage to the OUT pin of the 723 IC, V_{OUT} is a little bit greaterin the experimental version than in the simulated version, for both minimum and maximum output voltage. Anyway the built-in Zener diode operates in its regulation region all the time.

Table 4

	k	R_1 [K]	R_2 [K]	V_O [V]	V_{OUT} [V]	I_{Q1}
1.	1	8.2	50	0.0028	8.212	33.7 µA
2.	0	8.2	50	7.073	15.423	1.57mA

As a whole, the circuit behaves as we expected, the practical results confirming the simulated ones.

Our adjustable from zero voltage regulator has the advantage of simplicity compared with the regulator with two 723 ICs. We need only one integrated circuit (not two) and no auxiliary negative voltage source. With our voltage regulator the adjustable output range is [0V, V_{REF}]. Even if our maximum output voltage is 7.15V, the necessary input voltage should be greater with V_Z=6V than for the standard low voltage regulator with 723 IC. Thus the unregulated input voltage should be greater than 9.5V+6V=15.5V.

IV. REGULATION PERFORMANCES

In order to validate our final circuit we measure some regulation performances as they are defined in the data sheet of LM723.

- Line regulation
- Load regulation
- Temperature coefficient of output voltage

The testing was conducting by SPICE simulation for two output voltages, V_{O1} = 5V and V_{O2} = 0.5V for the voltage regulator with two 723 ICs [3] and for our voltage regulator. The results for line regulation are presented in Table 5 for both voltage regulators: the voltage regulator with two LM723 and our voltage regulator. The input voltage variation is 3V, the output current is 100 mA, load resistance R_l=50 Ω for V_O=5V and R_l=5 Ω for V_O = 0.5V.

Table 5

Test at V_O	V_I [V]	Voltage regulator with two LM723		Our voltage regulator	
		V_O [V]	ΔV_O %	V_O [V]	ΔV_O %
5V	18	4.999972440	0.005117	5.008471051	0.00438255
	21	5.000228289		5.008690550	
0.5V	18	0.5002561242	0.0182135	0.5003160283	0.04414367
	21	0.5003472387		0.5005368862	

Table 6

Test at V_O	Io [mA]	Voltage regulator with two LM723		Our voltage regulator	
		V_O [V]	ΔV_O %	V_O [V]	ΔV_O %
5V	99.99944880	4.999972440	0.00331203	5.008471051	0.00313532
	499.9806839	4.999806839		5.008314019	
0.5V	100.0512248	0.5002561242	0.01145487	0.5003160283	0.03059802
	500.1988205	0.5001988205		0.5001629415	

Table 7

Test at V_O	Temp [^{o}C]	Voltage regulator with two LM723		Our voltage regulator	
		V_O [V]	ΔV_O %	V_O [V]	ΔV_O %
5V	27	4.999972440	0.0297857	5.008471051	0.00504129
	100	5.001461720		5.008723543	
0.5V	27	0.5002561242	0.0905770	0.5003160283	0.05733721
	100	0.5007092412		0.5006028956	

The line regulation is similar for the two tested regulator with a small plus for our regulator at V_O=5V (0.00438255 compared with 0.005117), but with a small minus for our regulator at V_O=0.5V (0.04414367 compared with 0.0182135).

Table 6 contains the simulation results for the load regulation for both regulators. The input voltage is 18V and the output currents are I_{O1} = 100 mA and I_{O2} = 500 mA.

The load regulation is similar for the two tested regulator with a small plus for our regulator at V_O=5V (0.00313532 compared with 0.00331203), but with a small minus for our regulator at V_O=0.5V (0.03059802 compared with 0.01145487).

As one can see for V_O=5V our regulator has a little bit smaller values for regulation line and load regulation, while for V_O=0.5V our regulator has a little bit higher values for line and load regulation.

The results of simulation regarding the temperature coefficient of output voltage are presented in Table 7. The input voltage is 18V, and the rest of conditions are as for the line regulation case, the two values of temperature being 27^{o}C and 100^{o}C.

From the point of view of the dependence of the output voltage on the temperature our voltage regulator is better presenting a smaller variation of the output voltage with the temperature. For V_O=5V our regulator presents a relative variation of V_O with almost one magnitude order less than the one for the regulator with two 723 ICs (0.00504129 compared with 0.0297857). Also for V_O=0.5V our regulator presents a lower relative variation of V_O (0.05733721 compared with 0.0905770).

As a whole our adjustable from zero voltage regulator exhibit very good regulation parameters, being at the same level with the regulator with two ICs for the line and load regulation and superior for the temperature coefficient.

V. CONCLUSION

It has been shown in this paper how an adjustable from zero voltage regulator can be obtained.

The output voltage can be adjusted down to some mV that can be considered as low as zero for a voltage regulator, and up to V_{REF}. Because we use the built in Zener diode to raise the output voltage of the error amplifier we need at least 15.5V unregulated input voltage source. The results obtained by SPICE simulation shows very good performances of our voltage regulator. From the point of view of regulation performances our regulator has similar performances for line and load regulation as the performances of the existing solution with two 723ICs. From the point of view of temperature dependence our regulator is superior presenting smaller output voltage variations with the temperature than the regulator with two 723ICs.

Also, compared with the existing solution, our solution is advantageous because involves only one 723IC and no auxiliary negative voltage source.

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