ADJUSTABLE FROM ZERO VOLTAGE REGULATOR USING ONLY ONE 723 INTEGRATED CIRCUIT

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I. INTRODUCTION

The 723 IC is a flexible, easy-to-use voltage regulator with excellent performances [1]. It is really a power supply kit, containing temperature-compensated voltage reference \(V_{\text{REF}}\), differential amplifier, series pass transistor, Zener diode and current-limiting protective circuit. Using some external components the versatile 723 IC can be use to build a large variety of fixed and adjustable regulated voltage: basic low voltage regulator, basic high voltage regulator, positive and negative voltage regulator, positive and negative floating regulator, positive and negative switching regulator [2].

A particular attention should be paid if we want to build a positive voltage regulator adjustable from zero, as long as in the datasheet the adjustable output voltage is from 2V to 37V [2]. One solution uses two 723 ICs and an extra negative input voltage source [3].

The purpose of this paper is to analyze a solution that use only one 723 IC to build an adjustable from zero voltage regulator. We started with one initial circuit configuration and using SPICE simulations we improved it to the final configuration. Our idea has three distinct characteristics:

- keeps the output of the error amplifier above 2V, using the built-in Zener diode;
- keeps both inverting and non-inverting inputs of the error amplifier above 2V even for zero output voltage using resistive voltage dividers between reference voltage and output voltage and respectively between reference voltage and ground;
- uses a “smart” ballast equivalent resistance with a low value for minimum output voltage but with a high value for higher output voltages.

The remainder of the paper is organized as follows. Section II presents the internal simplified structure of 723IC, the basic circuit for the low voltage regulator and the existing solution for a zero volts adjustable from zero voltage regulator using two 723ICs. In Section III our idea is presented using only 723IC and no auxiliary negative voltage source. By means of SPICE simulation we analyze the behavior and performances of each circuit configurations. Section IV is concerned with the validation of our final circuit. We compare its regulation performances with the regulation performances of the existing solution. The regulation performances are obtained by SPICE simulation for both regulators. Finally, some conclusions are drawn in Section V.

II. THE EXISTING SOLUTION FOR ZERO LEVEL ADJUSTMENT

The equivalent circuit of LM 723 is presented in Fig.1. [2].

![Fig.1. The LM723 voltage regulator](image-url)
We can see that the $V_{\text{REF}}$ appears from pin 4 to pin 5, the same with the negative supply pin of error amplifier ($V_-$). The well known basic low voltage regulator in the range $V_O \in [2V; V_{\text{REF}}]$ is presented in Fig.2.

The internal LM 723 structure is still simplified: $V_{\text{REF}}$ is represented as a voltage source and the internal current limiter transistor is omitted. The expression of $V_O$ is:

$$V_O = \frac{(1-k)P + R}{P + R} V_{\text{REF}} \quad (1)$$

The $P, R$ voltage divider is sized to provide $V_{\text{Omin}} = V_{\text{IN}} = V_B \leq 2V$. As we know this is necessary to assure enough voltage to keep a series of bipolar transistor (not shown in Fig. 2) inside of IC in their active region for a proper operation of the error amplifier.

So, we cannot use the circuit in Fig.2. to adjust the output voltage to zero as long as we must keep the voltages to the inputs and output of the error amplifier (EA) greater to at least 2V than the potential of its negative supply $V_-$. The known solution [3] for zero volts adjustment using 723 IC uses the main idea to connect the negative supply of the amplifier ($V^*$) to a negative potential, less or equal with -2V. The principle of this solution is illustrated in Fig.3.

The auxiliary negative voltage $-V_a$ is regulated with an auxiliary LM 723 and an auxiliary input voltage $v_{Ia}$. $V_O$ can be easily deduced as:

$$V_O = -\frac{kP}{(1-k)P + R} (-V_a) = \frac{kP}{(1-k)P + R} V_a \quad (2)$$

For $k = 0$, $V_O = 0V$.

The disadvantage of this scheme is its complexity meaning the auxiliary voltage regulator to regulate $-V_a$ and the auxiliary input voltage source.

**III. OUR SOLUTION**

Our idea is to build a simpler voltage regulator, adjustable from zero, using only one 723 IC and no auxiliary negative voltage source.

**III. 1. The initial circuit configuration**

In order to prevent the inputs and output of the error amplifier to reach values below 2V we propose the initial circuit configuration presented in Fig. 4.
We use the integrated Zener diode ZD taking the output from the anode of the ZD instead from the emitter of integrated transistor. This way even for $V_O = 0\,\text{V}$ the output of the error amplifier has a potential raised with $V_{Z} + V_{Ref,\text{in}}$ in respect with the $V$ potential. As long as $V_Z \approx 6\,\text{V}$, the output of the error amplifier is well solved, with the condition to keep ZD in its regulated region, meaning enough $I_Z$ current. This is why we need a ballast resistor $R_b$ to assure a path for the $I_{Q1}$ current (so implicitly for $I_Z$ current), even in the absence of the load.

The negative feedback is assumed by the $R_b$, $R_i$ voltage divider, with its intermediate point connected to the inverting input of the error amplifier. The trick here is we do not connect the end of the divider to the ground, but to a positive stabilized voltage, $V_{REF}$. All we have to do further is to size the $R_b$, $R_i$ divider so that $V_{IL} \geq 2\,\text{V}$ for $V_O = 0\,\text{V}$.

The $V_O$ expression is straightforward to deduce:

$$V_O = V_{REF}\left[\frac{(1-k)P+R}{P+R} \cdot \frac{R_3+R_4}{R_3} - \frac{R_4}{R_3}\right]$$  \hspace{1cm} (3)

For $k = 0$, $V_{IN} = V_R = V_{REF}$, so voltage drop across $R_i$, so $V_O = V_{REF}$.

For $k = 1$ we expect $V_O = 0\,\text{V}$. From relation (3) results:

$$\frac{R}{P+R} = \frac{R_4}{R_3 + R_4}$$  \hspace{1cm} (4)

and also from condition of $v_{IN} = V_{IL} \geq 2\,\text{V}$ for worst case situation ($V_{REF} = V_{REF\text{max}}$):

$$\frac{P}{P+R} V_{REF\text{ min}} \geq 2\,\text{V}$$  \hspace{1cm} (5)

When we adjust the output voltage, the $I_I$ current will vary, so in order to keep constant $V_{REF}$, meaning constant $I_{REF}$ (see data sheet) we place the condition: $I_I > 10 I_S$, or:

$$R + P < \frac{1}{10} (R_3 + R_4)$$  \hspace{1cm} (6)

An extra design equation can be obtained by imposing the current through $V_{REF}$ (less than 15mA according to the data sheet). For $I_{REF} \approx 5\,\text{mA}$ the following relation appears:

$$\frac{V_{REF}}{R+P} = 5\,\text{mA}$$  \hspace{1cm} (7)

Using the design equation (4) - (7) we sized the resistances: $I = 1\,\text{KΩ}$, $I = 410\,\text{Ω}$, $I = 20\,\text{KΩ}$ and $I = 8.2\,\text{KΩ}$.

In order to analyze the behavior of the proposed configuration we conducted some SPICE simulations for different ballast resistance. The numerical results are presented in Table 1.

<table>
<thead>
<tr>
<th>$k$</th>
<th>$R_b$</th>
<th>$V_O$ [V]</th>
<th>$V_{OUT}$ [V]</th>
<th>$I_{Q1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1KΩ</td>
<td>0.1182</td>
<td>6.390</td>
<td>1.8μA</td>
</tr>
<tr>
<td>0</td>
<td>1KΩ</td>
<td>7.1632</td>
<td>13.8690</td>
<td>14.3mA</td>
</tr>
<tr>
<td>3</td>
<td>100Ω</td>
<td>0.0253</td>
<td>6.4435</td>
<td>40.66μA</td>
</tr>
<tr>
<td>4</td>
<td>100Ω</td>
<td>7.1663</td>
<td>13.9580</td>
<td>78.84mA</td>
</tr>
<tr>
<td>5</td>
<td>10Ω</td>
<td>0.0047</td>
<td>6.5064</td>
<td>233μA</td>
</tr>
<tr>
<td>6</td>
<td>10Ω</td>
<td>7.1666</td>
<td>14.0850</td>
<td>724mA</td>
</tr>
</tbody>
</table>

We can see that the minimum output voltage $V_O$ and the current through the external pass transistor $I_{Q1}$ depends on the $R_b$ value. Also from all $R_b$ and $k$ values we can see that the value of $V_{OUT}$ demonstrates that the Zener diode is in its regulation region. In order to obtain the lowest possible output voltage ($k = 1$) we must have a low value of $R_b$. For $R_b = 10\,\text{Ω}$, $k=1$, $V_{O\text{min}} = 4.7\,\text{mV}$ (row 5). It is a small enough value to consider that output voltage $V_O$ can be adjusted down to zero. When we set $k = 0$, $V_{O\text{min}} = 7.166 \,\text{V}$ (row 6) the current through $Q_1$ is very high $I_{Q1} = 724 \,\text{mA}$. This is not acceptable, because it is not a useful current, it increases very much the current consumption from the input source. For a higher $R_b$ value, $R_b = 1 \,\text{KΩ}$ (for $k = 0$), the maximum $I_{Q1}$ current decreases to $14.3 \,\text{mA}$ (row 2), still a high value, but the minimum output voltage increases up to $118.2 \,\text{mV}$ (row 1). The $V_{O\text{min}}$ increases with $R_b$ because the $I_I$ current must flow through $R_b$ resistor.

One solution to decrease $V_{O\text{min}}$ can be to decrease $I_I$ current by increasing $R_i$ and $R_b$ resistances. Anyway we can not decrease to much the $I_I$ current because it can reach a level comparable with the input bias current of error amplifier, so the $R_i$, $R_b$ will not act anymore as a simple voltage divider.

Returning to $R_b$ we can state: we need a low $R_b$ value when we set minimum $V_O$ but we need a high $R_b$ value when we set higher $V_O$. So, we need a “smart” resistor that “know” when $V_O$ is very low or high.

### III.2. Improved configuration

As a “smart” resistor we use the group $R_o$, $Q_o$, $Q_b$, $R_i$ and $R_2$ as one can see in Fig.5.

How does this group work? When $k$ is set towards 1 $V_O$ has a high value (towards $V_{REF}$). The $Q_1$ transistor goes into saturation and by the way of consequence $Q_2$ is off. So, the equivalent ballast resistance is formed by $R_b$ in parallel with $R_2$ plus the equivalent base-emitter d.c. resistance of $Q_2$.

With appropriate resistors value we can set a high enough equivalent resistance.

When $V_O$ decreases, the base current of $Q_1$ also decreases and $Q_1$ moves from the saturation towards the active region. At one moment (depending on the $R_i$ and $R_2$ values) $Q_2$ will be in its active region. When $V_O$ decreases below approximately 0.6V $Q_2$ will be turned off. On the other hand when $Q_2$ is not saturated, $Q_2$ can enter in the active region and draw a nonzero $I_{Q2}$ current from the output. When $V_O$ drop below 0.2V $Q_2$ enters in saturation, so it has a very low collector-emitter equivalent resistance and in conclusion very low ballast resistance.
We simulated this circuit for different combinations of the $R_1$ and $R_2$ values. The results are presented in Table 2.

<table>
<thead>
<tr>
<th>$k$</th>
<th>$R_1$ [K]</th>
<th>$R_2$ [K]</th>
<th>$V_O$ [V]</th>
<th>$V_{OUT}$ [V]</th>
<th>$I_{Q1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>10</td>
<td>0.0151</td>
<td>6.4813</td>
<td>111μA</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>10</td>
<td>7.1563</td>
<td>13.7830</td>
<td>2.89mA</td>
</tr>
<tr>
<td>3</td>
<td>0.93</td>
<td>10</td>
<td>0.5138</td>
<td>7.3380</td>
<td>155.1mA</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>10</td>
<td>0.0109</td>
<td>6.54107</td>
<td>420μA</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>10</td>
<td>7.0644</td>
<td>13.6900</td>
<td>2.85mA</td>
</tr>
<tr>
<td>6</td>
<td>0.88</td>
<td>10</td>
<td>0.8552</td>
<td>7.7451</td>
<td>490.1mA</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>10</td>
<td>0.0151</td>
<td>6.4813</td>
<td>111.1μA</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>10</td>
<td>7.1562</td>
<td>13.8360</td>
<td>8.661mA</td>
</tr>
<tr>
<td>9</td>
<td>0.93</td>
<td>10</td>
<td>0.5138</td>
<td>7.3380</td>
<td>155mA</td>
</tr>
</tbody>
</table>

From Table 2 one can observe we can obtain very low values of $V_O$ (15mV, 10mV, for $k = 1$) and also the $I_{Q1}$ value are acceptable (2.9mA or 8.6mA) for $V_{Omax}$ (k = 0). The equivalent ballast resistance behaves as we expected: low value for $V_{Omin}$ and high value for $V_{Omax}$.

A parametric analysis of $I_{Q1}$ value as a function of $k$ value ($V_O$ value) show us that the maximum $I_{Q1}$ current appears at a $V_O$ value for that the $Q_2$ transistor is in the active region. For example in rows 3 and 9 for $k = 0.93$, $V_O = 514$ mV results $I_{Q1} = 155$ mA. Or even worse $I_{Q1}$ reaches 490 mA for $R_1 = 1\, \Omega$, $R_2 = 10\, \Omega$, $k = 0.88$, $V_O = 855$ mV.

We have solved one problem (we reduced to an acceptable level the $I_{Q1}$ for $V_{Omax}$) but a new problem appears: high $I_{Q1}$ value for a certain $V_O$ value (depending on $R_1$ and $R_2$ values). The high $I_{Q2}$ value appears for active region of $Q_2$ as a consequence of the collector current $I_{Q2}$. This value is:

$$I_{Q2} = \beta \cdot \frac{V_{REF} - V_{BEon2}}{R_1}$$  

where $\beta$ is the d.c. current gain of the $Q_2$ transistor.

One way to reduce $I_{Q2}$ is to increase $R_1$, but doing this we increase the $V_{Omax}$ (10.9 mV for $R_1 = 1\, \Omega$, 15.1 mV for $R_1 = 10\, \Omega$), so this is not a very good idea.

A better idea is to use a transistor with a low $\beta$ value, the idea that is analyzed in the next paragraph.

**III.3. The final configuration**

We know that a transistor can be also used in the reverse active region, where its current gain $\beta_k$ is much smaller that the one in the active region. So, the great idea is to reverse the $Q_2$ transistor so that when in active reverse region it will work with a very low current gain.

<table>
<thead>
<tr>
<th>$k$</th>
<th>$R_1$ [K]</th>
<th>$R_2$ [K]</th>
<th>$V_O$ [V]</th>
<th>$V_{OUT}$ [V]</th>
<th>$I_{Q1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>10</td>
<td>0.0082</td>
<td>6.4451</td>
<td>824nA</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>10</td>
<td>7.1565</td>
<td>13.7830</td>
<td>2.896mA</td>
</tr>
<tr>
<td>3</td>
<td>0.93</td>
<td>10</td>
<td>0.5077</td>
<td>7.0904</td>
<td>1.241mA</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>10</td>
<td>0.0109</td>
<td>6.5190</td>
<td>266μA</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>10</td>
<td>7.0644</td>
<td>13.6900</td>
<td>2.855mA</td>
</tr>
<tr>
<td>6</td>
<td>0.93</td>
<td>10</td>
<td>0.5042</td>
<td>7.208</td>
<td>14.73mA</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>10</td>
<td>0.0082</td>
<td>6.4451</td>
<td>60.1μA</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>10</td>
<td>7.1564</td>
<td>13.8370</td>
<td>8.66mA</td>
</tr>
<tr>
<td>9</td>
<td>0.93</td>
<td>10</td>
<td>0.5077</td>
<td>7.0904</td>
<td>1.241mA</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>50</td>
<td>0.0067</td>
<td>6.2849</td>
<td>2.12u</td>
</tr>
<tr>
<td>11</td>
<td>0</td>
<td>50</td>
<td>7.1566</td>
<td>13.7730</td>
<td>2.379m</td>
</tr>
<tr>
<td>12</td>
<td>0.93</td>
<td>50</td>
<td>0.4349</td>
<td>7.0168</td>
<td>1.241m</td>
</tr>
</tbody>
</table>

The final, complete scheme is shown in Fig.6. The extra potentiometer $P_Z$ is necessary to make the zero volts adjustment.
In Table 3 some numerical results obtained by SPICE simulation for different \( R_1 \) and \( R_2 \) values combination are presented. The numerical results show good performance of our adjustable from zero voltage regulator. Regardless the \( R_1 \) and \( R_2 \) values the \( V_{\text{ou}} \) has a very good value, less than 10 mV (even 6.7 mV, in row 10). This value can be considered as low as zero for a voltage regulator. The maximum value of the \( I_{Q1} \) current is below 3 mA in all but one situation, so no important extra current for proper operation of voltage regulator is necessary.

We can observe the drastically reduction of maximum \( I_{Q1} \) due to the operation of \( Q_2 \) in reverse region. For example, for \( R_1 = R_2 = 10K \Omega \) and \( k = 0.93 \), \( I_{Q1} \) was reduced from 155 mA with \( Q_2 \) in forward active region (row3 in Table 2) up to 1.24 mA with \( Q_2 \) in reverse active region (row3 in Table 3). It is important to note that the maximum \( I_{Q1} \) current appears for \( V_{\text{ou}} \) when \( Q_2 \) is saturated, not for \( Q_2 \) in active region. This happens for all situations where \( R_1 \neq 1K \Omega \).

As optimal solution we choose the last one in Table 3, \( R_1=10K \Omega \), \( R_2=50K \Omega \) that provide \( V_{\text{ou}}=6.7 \) mV and \( I_{Q1\text{max}}=2.38 \) mA.

The final version of the voltage regulator was also practically implemented. For better results, a small adjustment was necessary for the \( R_1 \) resistor value (8.2K\( \Omega \) instead of 10K\( \Omega \)). The experimental results are presented in Table 4.

The minimum output voltage \( V_{\text{ou}}=2.8mV \) is even better than the value obtained by simulation (6.7mV). The maximum output voltage \( V_{\text{ou\text{max}}} \) is quite the same with the simulated one (7.1566V). For the maximum output voltage the current through \( Q_1 \) is 1.57 mA, meaning low current necessary for the equivalent ballast resistor. The voltage to the OUT pin of the 723 IC, \( V_{\text{OUT}} \) is a little bit greaterin the experimental version than in the simulated version, for both minimum and maximum output voltage. Anyway the built-in Zener diode operates in its regulation region all the time.

As a whole, the circuit behaves as we expected, the practical results confirming the simulated ones. Our adjustable from zero voltage regulator has the advantage of simplicity compared with the regulator with two 723 ICs. We need only one integrated circuit (not two) and no auxiliary negative voltage source. With our voltage regulator the adjustable output range is [0V, \( V_{\text{REF}} \)]. Even if our maximum output voltage is 7.15V, the necessary input voltage should be greater with \( V_\text{in}=6V \) than for the standard low voltage regulator with 723 IC. Thus the unregulated input voltage should be greater than 9.5V+6V=15.5V.

### IV. REGULATION PERFORMANCES

In order to validate our final circuit we measure some regulation performances as they are defined in the data sheet of LM723:

- Line regulation
- Load regulation
- Temperature coefficient of output voltage

The testing was conducting by SPICE simulation for two output voltages, \( V_{\text{O1}} = 5V \) and \( V_{\text{O2}} = 0.5V \) for the voltage regulator with two 723 ICs [3] and for our voltage regulator. The results for line regulation are presented in Table 5 for both voltage regulators: the voltage regulator with two LM723 and our voltage regulator. The input voltage variation is 3V, the output current is 100 mA, load resistance \( R_L=50 \Omega \) for \( V_{\text{O2}}=5V \) and \( R_L=5 \Omega \) for \( V_{\text{O}} = 0.5V \).
The line regulation is similar for the two tested regulator with a small plus for our regulator at \( V_O=5\)V (0.00438255 compared with 0.005117), but with a small minus for our regulator at \( V_O=0.5\)V (0.04414367 compared with 0.0182135).

Table 6 contains the simulation results for the load regulation for both regulators. The input voltage is 18V and the rest of conditions are as for the line regulation case, the two values of temperature being 27°C and 100°C.

As one can see for \( V_O=5\)V our regulator has a little bit smaller values for regulation line and load regulation, while for \( V_O=0.5\)V our regulator has a little bit higher values for line and load regulation.

The results of simulation regarding the temperature coefficient of output voltage are presented in Table 7. The input voltage is 18V, and the rest of conditions are as for the line regulation case, the two values of temperature being 27°C and 100°C.

From the point of view of the dependence of the output voltage on the temperature our voltage regulator is better presenting a smaller variation of the output voltage with the temperature. For \( V_O=5\)V our regulator presents a relative variation of \( V_O \) with almost one magnitude order less than the one for the regulator with two 723 ICs (0.00504129 compared with 0.0297857). Also for \( V_O=0.5\)V our regulator presents a lower relative variation of \( V_O \) (0.05733721 compared with 0.0905770).

As a whole our adjustable from zero voltage regulator exhibit very good regulation parameters, being at the same level with the regulator with two ICs for the line and load regulation and superior for the temperature coefficient.

V. CONCLUSION

It has been shown in this paper how an adjustable from zero voltage regulator can be obtained.

The output voltage can be adjusted down to some mV that can be considered as low as zero for a voltage regulator, and up to \( V_{REF} \). Because we use the built in Zener diode to raise the output voltage of the error amplifier we need at least 15.5V unregulated input voltage source. The results obtained by SPICE simulation shows very good performances of our voltage regulator. From the point of view of regulation performances our regulator has similar performances for line and load regulation as the performances of the existing solution with two 723ICs. From the point of view of temperature dependence our regulator is superior presenting smaller output voltage variations with the temperature than the regulator with two 723ICs.

Also, compared with the existing solution, our solution is advantageous because involves only one 723IC and no auxiliary negative voltage source.

REFERENCES